WHAT IS CLAIMED IS:

1. A semiconductor chip comprising:

a plurality of outer edges;

a peripheral area located adjacent to the outer edges; and

a main circuit area located within the confines of the peripheral area, the main circuit area including integrated circuits,

wherein the peripheral area includes chip pads connected to the integrated circuits, and also a plurality of test pads electrically connected to the integrated circuits for testing electrical properties of the integrated circuits.

2. The semiconductor chip of claim 1, wherein the chip pads are arranged in rows adjacent the main circuit area of the semiconductor chip, and the test pads are located within the rows of chip pads.

3. The semiconductor chip of claim 1, wherein the chip pads and the test pads are arranged at substantially uniform intervals.

4. The semiconductor chip of claim 2, wherein the test pads are located at the ends of the rows of chip pads.

5. The semiconductor chip of claim 2, wherein the configuration of the main circuit area is arranged to form corners, and the test pads are located near the corners of the main circuit area.

6. The semiconductor chip of claim 1, wherein the chip pads are arranged in rows parallel to at least one set of opposed outer edges of the semiconductor chip, and the test pads are arranged within the rows of chip pads.

7. The semiconductor chip of claim 2, wherein the test pads are arranged between chip pads within the rows of chip pads.

8. The semiconductor chip of claim 1, wherein the test pads are substantially the same dimensional size as the chip pads.

9. The semiconductor chip of claim 1, wherein the test pads are mounted by bump bonding.

10. The semiconductor chip of claim 1, which comprises one of an edge-pad-type chip and a center-pad-type chip.

11. A tape carrier package comprising:

a semiconductor chip comprising a plurality of outer edges, a peripheral area located adjacent to the outer edges, and an main circuit area located within the confines of the peripheral area, the main circuit area including integrated circuits, the peripheral area including chip pads connected to the integrated circuits, and a plurality of test pads electrically connected to the integrated circuits for testing the electrical properties of the integrated circuits; and

a tape wiring substrate.

12. The tape carrier package of claim 11, wherein the chip pads are arranged in rows adjacent the main circuit area of the semiconductor chip, and the test pads are located within the rows of chip pads.

13. The tape carrier package of claim 11, wherein the chip pads and the test pads are arranged at substantially uniform intervals.

14. The tape carrier package of claim 12, wherein the test pads are located at the ends of the rows of chip pads.

15. The tape carrier package of claim 12, wherein the configuration of the main circuit area is arranged to form corners, and the test pads are located near the corners of the main circuit area.

16. The tape carrier package of claim 11, wherein the chip pads are arranged in rows parallel to at least one set of opposed outer edges of the semiconductor chip, and the test pads are arranged within the rows of chip pads.

17. The tape carrier package of claim 12, wherein the test pads are arranged between chip pads within the rows of chip pads.

18. The tape carrier package of claim 11, wherein the test pads are substantially the same dimensional size as the chip pads.

19. The tape carrier package of claim 11, wherein the tape wiring substrate comprises an insulating base film, wiring patterns formed on the insulating base film, leads formed integrally with the wiring patterns, and dummy leads electrically isolated from the wiring patterns.

20. The tape carrier package of claim 19, which further comprises bumps connecting the chip pads to the corresponding leads and the test pads to the dummy leads.